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EXAMINER

CHERY, MARDOCHEE

ART UNIT	PAPER NUMBER
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2188

DATE MAILED: 07/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/091,766

Applicant(s)

MCCLAIN, MARK ALAN

Examiner

Mardochee Chery

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 13 April 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-23 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-23 is/are rejected.
- 7) ☒ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 13 April 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Response to Amendment

1. This Office Action is in response to applicant's communication filed on April 13, 2005, in response to PTO Office Action mailed on January 14, 2005. The applicant's remarks and amendments to the claims and/or the specification were considered with the results that follow.
2. Claims 1-23 have been presented for examination in this application. In response to the PTO Office Action mailed on January 14, 2005, claim 1 has been amended. No claims have been added or canceled. As a result, claims 1-23 remain pending in this application.
3. The objection to the Drawings has been withdrawn due to the amendment filed on April 13, 2005.
4. The rejection of claims 1-23, in view of the new ground, is laid out below for applicant's convenience.

Response to Arguments

5. Applicant's arguments, filed on April 13, 2005, with respect to claim 1 have been considered but are moot in view of the new ground(s) of rejection.

6. Applicant's arguments, filed on April 13, 2005, see page 10, par.3, page 14, par.2, and page 16, par.2, filed April 13, 2005, with respect to the rejection(s) of claim(s) 3, 6, 20, under 35 USC 102 (b), and claim 5, under 35 USC 102 (e), have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of the cited prior art.

Applicant argues on page 15, paragraph 3 that Zarrin does not anticipate or render obvious "a computer system that includes non-volatile memory and SDRAM, wherein the non-volatile memory shares a common interface with SDRAM " because Zarrin teaches [a processor coupled to a volatile memory and a non-volatile memory via a bus; col.4, lines 19-22]. Applicant further argues, "a bus is only part of an SDRAM interface, not a complete interface."

Examiner completely disagrees. Examiner would like to point out that the bus disclosed in the system of Zarrin fully effects the function of an interface between two memory devices, mainly transferring address, data, and transmit signals across such. Furthermore, the broadest interpretation is given to the word "interface" since it was not defined otherwise in the specification.

7. Therefore the rejection of claims 1-23, in view of the new ground, is laid out below for applicant's convenience.

Claim Objections

8. Claims 4 and 6 are objected to because of the following informalities:

- a. In claim 4, line 3, "is " should be changed to --are--.
- b. In claim 6, line 8, "a" should be changed to --at--.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

9. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

10. Claim 1 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The following points out where in the claim such limitations are found which fail the written description requirement:

- (1) At line 4, "SDRAM style address lines".

(2) At line 6, "SDRAM style sequential access logic".

(3) At line 8, "SDRAM style control signals".

Therefore, the broadest reasonable interpretation will be given when analyzing the claim in view of the prior art.

Claim Rejections - 35 USC § 102

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

12. Claims 2 and 10 is rejected under 35 U.S.C. 102(e) as being anticipated by Zarrin et al. (6,128,731).

As per claims 2 and 10, Zarrin et al. discloses a computer system that includes non-volatile memory and SDRAM, the non-volatile memory shares a common interface with SDRAM [*the computer system includes one or more processors coupled to a volatile memory (e.g., SDRAM) and a non-volatile memory (e.g., flash memory) via one or more buses; col.4, lines 19-22*].

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13. Claim 5 is rejected under 35 U.S.C. 102(e) as being anticipated by Wisor (6,823,435).

As per claim 5, Wisor discloses a method of reducing control and address lines in a computer system having non-volatile memory and SDRAM [*the non-volatile memory cells are accessed using address signals driven upon the address lines of memory bus 20; col.4, lines 58-60*].

14. Claims 3-4, and 6-23, are rejected under 35 U.S.C. 102(e) as being anticipated by Gibson et al. (6,601,167).

As per claim 3, Gibson et al. discloses a method of initializing a computer system [*the boot loader includes a state machine, which in response to initialization of the computer system; col.2, lines 25-26*]; reading boot code stored in a non-volatile memory [*read the first page of sequential memory (Flash memory, EEPROM) containing a first portion of the boot program; Fig.8; Sequential Access Memory 32; col.2, lines 27-29*]; the first memory location in the non-volatile memory is read using at least one control signal that functions independently of the SDRAM style interface [*the boot program is configured to control the processor to transfer boot code from the sequential access memory to a volatile Random Memory (RAM) using move immediate instructions; col.14, lines 37-41; the computer system controls the sequential access memory to read the first page of sequential memory containing a first portion of the boot program; col.2, lines 26-29*].

As per claim 4, Gibson et al. discloses subsequent memory locations are read by means of at least one control signal that functions independently of the SDRAM style interface and is received by sequential access logic incorporated in the non-volatile memory [*the computer system controls the sequential access memory to read the first page of sequential memory containing a first portion of the boot program*; col.2, lines 26-29].

As per claim 6, Gibson et al. discloses a method of configuring a SDRAM interface in a computer system [*initial program execution must occur in the non-volatile ROM at least until the sequential access memory has been set up for reading and programs in the sequential access memory can be transferred to volatile Random Access Memory (RAM)*; col.2, lines 2-6]; the computer system has a non-volatile memory with a SDRAM style interface [*the boot is configured to control the processor to transfer boot code from the sequential access memory to a volatile Random Memory (RAM)*; col.13, lines 32-35]; storing interface initialization code starting at the first location in the first accessed memory row of the non-volatile memory [*computer system includes a non-volatile Read Only Memory (ROM) which contains boot code instructions*; col.1, lines 17-19; *a sequential access memory having a boot program stored therein*; col.2, lines 23-24]; providing at least one control signal independent of the SDRAM style interface for incrementing the internal address of the non-volatile memory [*the boot loader includes a state machine, which in response to initialization of the computer system controls the sequential access memory to read the first page of sequential memory containing a first portion of the boot program*; col.2, lines 25-29]; providing at least one control signal independent of the SDRAM style interface for performing a read operation from the first location in the first accessed memory row of the non-volatile memory [*the boot program is configured to control the processor*

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to transfer boot code from the sequential access memory to a volatile Random Memory (RAM) using move immediate instructions; col.14, lines 37-41; the computer system controls the sequential access memory to read the first page of sequential memory containing a first portion of the boot program; col.2, lines 26-29].

As per claim 10, Gibson et. al. discloses a computer system, non-volatile memory, and volatile memory, the non-volatile memory and volatile memory have a common interface [*initial program execution must occur in the non-volatile ROM at least until the sequential access memory has been set up for reading and programs in the sequential access memory can be transferred to volatile Random Access Memory (RAM); col.2, lines 2-6].*

As per claim 20, Gibson et al. discloses, a computer system, a non-volatile memory having a SDRAM style interface [*the boot program is configured to control the processor to transfer boot code from the sequential access memory (Flash memory) to a volatile Random Memory (RAM); col.14, lines 37-41].*

As per claim 7, Gibson et al. discloses the interface initialization code performs no branch operations [*the boot code stored in the flash device will not cause the micro-controller to branch or jump either forward or backward; col.11, lines 20-22].*

As per claims 8 and 9, the rationale in the rejection of claim 6 above is herein incorporated. Gibson et al. further discloses a final instruction for branching to the system initialization code in the random access memory [*the system is configured to jump to a*

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predetermined memory address and begin executing the boot code upon initialization; col.1, lines 24-27].

As per claim 11, applicant's attention is directed to the rejection of claim 10 *supra*.

As per claims 12-13, 18-19, and 22-23, applicant's attention is directed to the rejection of claim 6 above.

As per claim 14, Gibson et al. discloses the interface initialization code for initializing the interface includes no branch operations until the system is ready to provide random access to memory [*once the second portion of the boot code is copied to RAM, the first portion of the boot code executes a branch (jump) instruction; col.2, lines 33-35*].

As per claim 15, applicant's attention is directed to the rejection of claim 3 *supra*.

As per claim 16, Gibson et al. discloses a copy instruction is included after the interface initialization code, for copying boot code to a random access memory, and a branch instruction is included after the copy instruction for branching to the copied code in the random access memory [*a boot code ROM in which an instruction or data at any address can be accessed; supports the branching behavior of most programs in which an instruction following a branch can be read; col.1, lines 30-34; initial program execution must occur in the non-volatile ROM at least until the sequential access memory has been set up for reading and programs in the sequential*

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access memory can be transferred to volatile Random Access Memory (RAM) for execution; col.2, lines 2-6].

As per claim 17, Gibson et al. discloses the interface initialization code is followed by a jump command to jump to a location in the non-volatile memory where the first instruction of at least part of the system boot code is stored *[the system is configured to jump to a predetermined memory address in the ROM and begin executing the boot code upon initialization of the system; col.1, lines 24-27].*

As per claim 21, Gibson et al. discloses the non-volatile memory is Flash memory *[the system code is stored in flash memory; col.6, lines 47-48; this memory is a flash ROM; col.1, lines 49-50].*

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

16. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fallon (6,748,457), in view of Dowling (6,226,738), Itomitsu (5,509,137), and further in view of Nakaoka (6,038,648).

As per claim 1, Fallon discloses a non-volatile memory comprising a memory interface wherein the memory interface requires initialization prior to use [*a non-volatile memory comprising a memory interface*; Abstract; *upon power-up or external reset, the interface 14 is initialized*; col.8, lines 6-8]; sequential access logic incorporated in a logic subsystem [*sequential access logic*; col.16, lines 44-49].

However, Fallon does not specifically teach the memory comprises an SDRAM style interface as recited in the claim.

Dowling discloses a SDRAM style interface [*a SDRAM style interface*; col.18, lines 24-25]; SDRAM style control signals to read a first address sequence, presented a second and subsequent address locations [*an interface responsive to address and control signals to transfer data between the DRAM and the external source*; col.5, lines 8-11] to transmit clock inputs and control signals (col.18, line 23).

Since the technology for implementing a memory system with a SDRAM style interface was well known as evidenced by Dowling and since a SDRAM style interface transmit clock inputs and control signals, an artisan would have been motivated to implement this feature in the system of Fallon. Thus, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant, to modify the system of Fallon to incorporate a SDRAM style interface because it was well known to transmit clock inputs and control signals (col.18, line 23) as taught by Dowling.

However, Fallon, and Dowling, do not specifically teach address lines multiplexed in time, wherein a least significant portion and a most significant portion of an address are presented sequentially in two successive stages as recited in the claim.

Itomitsu teaches address lines multiplexed in time, wherein a least significant portion and a most significant portion of an address are presented sequentially in two successive stages [*during first and second consecutive clock periods, a computer storing words at a plurality of addresses, each of the plurality of memory addresses consisting of a first portion and a second portion, the first portion consisting of the most significant bits, and the second portion consisting of the least significant bits*; col.18, lines 54-63] for storing a plurality of data words in a memory (col.18, line 53-54).

Since the technology for implementing a memory system with a least significant portion and a most significant portion of an address presented sequentially in two successive stages was well known as evidenced by Itomitsu and since a least significant portion and a most significant portion of an address presented sequentially in two successive stages is used to store a plurality of data words in a memory, an artisan would have been motivated to implement this feature in the system of Fallon and Dowling. Thus, it would have been obvious to one of ordinary skill in the art at the time of invention by Applicant to modify the system of Fallon and Dowling to incorporate a least significant portion and a most significant portion of an address presented sequentially in two successive stages because it was well known for storing a plurality of data words in a memory (col.18, line 53-54) as taught by Itomitsu.

However Fallon, Dowling, and Itomitsu do not specifically teach after a first address sequence is presented a second and subsequent address locations can be read using one or more additional control signals as recited in the claim.

Nakaoka discloses after a first address sequence is presented a second and subsequent address locations can be read using one or more additional control signals [a first address is generated in a sequential mode in response to a first control signal; a second and subsequent address is generated in response to a control signal based on control signals designating a read operation; Abstract] to provide synchronization with a clock signal (col.1, lines 10-11).

Since the technology for implementing a memory system wherein after a first address sequence is presented a second and subsequent address locations can be read using one or more additional control signals was well known as evidenced by Nakaoka and since after a first address sequence is presented a second and subsequent address locations can be read using one or more additional control signals provides synchronization with a clock signal, an artisan would have been motivated to implement this feature in the system of Fallon, Dowling, and Itomitsu. Thus, it would have been obvious to one of ordinary skill in the art at the time of invention by Applicant, to modify the system of Fallon, Dowling, and Itomitsu, to incorporate after a first address sequence is presented a second and subsequent address locations can be read using one or more additional control signals because it was well known to provide synchronization with a clock signal (col.1, lines 10-11) as taught by Nakaoka.

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17. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fallon (6,748,457), in view of Dowling (6,226,738).

As per claim 3, Fallon discloses a method of initializing a computer system [*boot configuration for controlling initialization of the computer system*; col.9, lines 56-58]; reading boot code stored in a non-volatile memory [*the boot loader code continues with executing the remainder of the code in the non-volatile memory device*; col.11, lines 34-36]; the first memory location in the non-volatile memory is read using at least one control signal that functions independently of the SDRAM style interface [*the first 1K of memory of the non-volatile memory device 24 is copied into internal RAM by the DMA*; col.11, lines 25-28; *using one or more signals, reading configuration data from the non-volatile memory*; col.14, lines 2-5].

However, Fallon does not specifically teach an SDRAM style interface as recited in the claim.

Dowling discloses a SDRAM style interface [*a SDRAM style interface*; col.18, lines 24-25] to transmit clock inputs and control signals (col.18, line 23).

Since the technology for implementing a memory system with a SDRAM style interface was well known as evidenced by Dowling and since a SDRAM style interface transmit clock inputs and control signals, an artisan would have been motivated to implement this feature in the system of Gibson. Thus, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant, to modify the system of Gibson to incorporate a SDRAM style interface because it was well known to transmit clock inputs and control signals (col.18, line 23) as taught by Dowling.

18. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fallon (6,748,457), in view of Dowling (6,226,738), and further in view of Stancil (5,951,685).

As per claim 4, Dowling is relied upon for the teaching of a SDRAM style interface as shown in claim 3. Dowling further discloses subsequent memory locations are read by means of at least one control signal that functions independently of the SDRAM style interface and is received by sequential access logic incorporated in the non-volatile memory [*an interface is responsive to address and control signals generated from an external source to transfer data between the DRAM and the external source*; col.5, lines 8-11; *a first interface accepts address and control information used to access the DRAM; a second interface receives information from an external source (i.e. including the non-volatile memory)*; col.7, lines 26-30].

However, Dowling does not specifically teach that subsequent memory locations are read and are received by sequential access logic incorporated in the non-volatile memory as recited in the claim.

Stancil discloses subsequent memory locations are read and are received by sequential access logic incorporated in the non-volatile memory [*sequential reading and accesses of serial access PROM*; col.5, lines 61-62; Figs. 2 – 4] to address and read the BIOS code stored in the non-volatile memory (col.5, lines 60-62).

Since the technology for implementing a memory system with subsequent memory locations read and received by sequential access logic incorporated in the non-volatile memory was well known as evidenced by Stancil and since subsequent memory

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locations read and received by sequential access logic incorporated in the non-volatile memory address and read the BIOS code stored in the non-volatile memory, an artisan would have been motivated to implement this feature in the system of Dowling. Thus, it would have been obvious to one of ordinary skill in the art at the time of invention by Applicant, to modify the system of Dowling to include sequential access logic incorporated in the non-volatile memory because it was well known to address and read the BIOS code stored in the non-volatile memory (col.5, lines 60-62) as taught by Stancil.

19. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Murakami (5,125,045), in view of Dowling (6,226,738).

As per claim 5, Murakami discloses a method of reducing control and address lines in a computer system having non-volatile memory and SDRAM [*reducing the number of address lines*; col.39, lines 1-2].

However, Murakami does not specifically teach the memory comprises an SDRAM style interface as recited in the claim.

Dowling discloses a SDRAM style interface [*a SDRAM style interface*; col.18, lines 24-25]; SDRAM style control signals to read a first address sequence, presented a second and subsequent address locations [*an interface responsive to address and control signals to transfer data between the DRAM and the external source*; col.5, lines 8-11] to transmit clock inputs and control signals (col.18, line 23).

Since the technology for implementing a memory system with a SDRAM style interface was well known as evidenced by Murakami and since a SDRAM style interface transmit clock inputs and control signals, an artisan would have been motivated to implement this feature in the system of Murakami. Thus, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant, to modify the system of Murakami to incorporate a SDRAM style interface because it was well known to transmit clock inputs and control signals (col.18, line 23) as taught by Dowling.

20. Claims 11-12, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zarrin (6,128,731) as applied to claim 10, and further in view of Fallon (6,748,457) and Dowling (6,226,738).

As per claim 11, Zarrin discloses the claimed invention as discussed above in the previous paragraphs. However Zarrin does not specifically teach the interface requires software-controlled initialization as recited in the claim.

Fallon discloses the interface requires software-controlled initialization [*the interface 14 is initialized*; col.8, lines 6-8] to initialize the interface upon power-up or reset (col.8, lines 6-8).

Since the technology for implementing a memory system with the interface requiring software-controlled initialization was well known as evidenced by Fallon and since the interface requiring software-controlled initialization initializes the interface upon power-up or reset, an artisan would have been motivated to implement this feature

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in the system of Zarrin. Thus, it would have been obvious to one of ordinary skill in the art, at the time of invention by applicant, to modify the system of Zaring to include an interface requiring software-controlled initialization because it was well known to initialize the interface upon power-up or reset (col.8, lines 6-8) as taught by Fallon.

However, Zarrin and Fallon do not specifically teach an SDRAM style interface as recited in the claim.

Dowling discloses a SDRAM style interface [*a SDRAM style interface*; col.18, lines 24-25] to transmit clock inputs and control signals (col.18, line 23).

Since the technology for implementing a memory system with a SDRAM style interface was well known as evidenced by Dowling and since a SDRAM style interface transmit clock inputs and control signals, an artisan would have been motivated to implement this feature in the system of Zarrin and Fallon. Thus, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant, to modify the system of Zarrin and Fallon to incorporate a SDRAM style interface because it was well known to transmit clock inputs and control signals (col.18, line 23) as taught by Dowling.

As per claim 12, Fallon discloses interface initialization code for initializing the interface is stored starting at the first memory location in the first accessed memory row of the non-volatile memory [*boot configuration controlling initialization*; col.9, lines 56-58; *the first 1K of memory of the non-volatile memory device 24 is copied by the DMA*; col.11, lines 25-28; *using one or more signals, reading configuration data from the non-volatile memory*; col.14, lines 2-5].

As per claim 15, Fallon discloses system boot code is stored in the non-volatile memory [*the boot loader code continues with executing the remainder of the code in the non-volatile memory device*; col.11, lines 34-36].

21. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zarrin (6,128,731) in view of Fallon (6,748,457), Dowling (6,226,738), and further in view of Itomitsu (5,509,137).

As per claim 17, Zarrin, Fallon and Dowling disclose the claimed invention as discussed above in the previous paragraphs. However, Zarrin, Fallon and Dowling do not specifically teach a jump command to jump to a location in the non-volatile memory where the first instruction of at least part of the system boot code is stored as recited in the claim.

Itomitsu discloses a jump command to jump to a location in the non-volatile memory where the first instruction of at least part of the system boot code is stored [*an instruction code following a conditional branch instruction*; col.4, lines 31-33] to jump to a plurality of data words stored in a memory (col.18, line 53-54).

Since the technology for implementing a memory system with a jump command to jump to a location in the non-volatile memory where the first instruction of at least part of the system boot code is stored was well known as evidenced by Itomitsu and since a jump command to jump to a location in the non-volatile memory jumps to a

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plurality of data words stored in a memory, an artisan would have been motivated to implement this feature in the system of Zarrin, Fallon and Dowling. Thus, it would have been obvious to one of ordinary skill in the art at the time of invention by Applicant to modify the system of Zarrin, Fallon and Dowling to incorporate a jump command to jump to a location in the non-volatile memory because it was well known to jump to a plurality of data words stored in a memory (col.18, line 53-54) as taught by Itomitsu.

22. Claims 20-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zarrin (6,128,731) in view of Dowling (6,226,738).

As per claim 20, Zarrin discloses a computer system that includes non-volatile memory [*the computer system includes one or more processors coupled to a volatile memory (e.g., SDRAM) and a non-volatile memory (e.g., flash memory) via one or more buses*; col.4, lines 19-22].

However, Zarrin does not specifically teach the non-volatile memory having a SDRAM style interface as recited in the claim.

Dowling discloses a SDRAM style interface [*a SDRAM style interface*; col.18, lines 24-25] to transmit clock inputs and control signals (col.18, line 23).

Since the technology for implementing a memory system with a SDRAM style interface was well known as evidenced by Dowling and since a SDRAM style interface transmit clock inputs and control signals, an artisan would have been motivated to implement this feature in the system of Zarrin. Thus, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant, to modify the system of

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Zarrin to incorporate a SDRAM style interface because it was well known to transmit clock inputs and control signals (col.18, line 23) as taught by Dowling.

As per claim 21, Zarrin discloses the non-volatile memory is a Flash memory [a *non-volatile memory (e.g., flash memory)*; col.4, lines 19-22].

23. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zarrin (6,128,731) in view of Dowling (6,226,738) and further in view of Fallon (6,748,457).

As per claim 22, Dowling is relied upon for the teaching of an SDRAM style interface as shown in claim 20. Zarrin and Dowling disclose the claimed invention as discussed above in the previous paragraphs. However, Zarrin and Dowling do not specifically teach interface initialization code for initializing the interface is stored starting at the first location in the first accessed memory row of the non-volatile memory as recited in the claim.

Fallon discloses interface initialization code for initializing the interface is stored starting at the first location in the first accessed memory row of the non-volatile memory [*boot configuration controlling initialization*; col.9, lines 56-58; *the first 1K of memory of the non-volatile memory device 24 is copied by the DMA*; col.11, lines 25-28; *using one or more signals, reading configuration data from the non-volatile memory*; col.14, lines 2-5] to facilitate the computer's boot-up sequence (col.8, lines 9-11).

Since the technology for implementing a computer system with storing interface initialization code starting at the first location in the first accessed memory row of the non-volatile memory was well known as evidence by Fallon, and since storing interface initialization code starting at the first location in the first accessed memory row of the non-volatile memory facilitates the computer's boot-up sequence, an artisan would have been motivated to implement this feature in the system of Zarrin and Dowling. Thus, it would have been obvious to one of ordinary skill in the art at the time of invention by Applicant, to modify the system of Zarrin and Dowling to incorporate storing interface initialization code starting at the first location in the first accessed memory row of the non-volatile memory because it was well known to facilitate the computer's boot-up sequence (col.8, lines 9-11) as taught by Fallon.

Conclusion

24. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Shiau	6,119,226
Iwasaki	4,760,524
Hirabayashi	6,295,596
Itomitsu	5,509,137
Murakami	5,125,045
Stancil	5,951,685
Nakaoka	6,038,648

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Dowling	6,226,738
Fallon	6,748,457
Fallon	2001/0052038
Gibson et al.	6,601,167
Zarrin et al.	6,128,731
Wisor	6,823,435
MacDonald	EP0691616
David V.James	Multiplexed Buses, June 1990 IEEE

25. When responding to the office action, Applicant is advised to clearly point out the patentable novelty that he or she thinks the claims present in view of the state of the art disclosed by references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. 1.111(c).

26. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

27. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mardochee Chery whose telephone number is (571) 272-4246. The examiner can normally be reached on 8:30A-5:00P.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Manonama Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

July 11, 2005


Mardochee Chery
Examiner
AU: 2188

 
7/11/05

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER